REMARKS

Reconsideration of the above-identified Application is respectfully requested. Claims 1 - 4 are in the case. Claims 1 and 2 have been canceled. Claim 3 has been amended.

Regarding the objection to Claims 3 and 4, the amendment to Claim 3, kindly suggested by the Examiner, has been made. Claim 3 has also been amended by replacing "second" with --first-- in line 9, to correct an inadvertent formal error. Accordingly, it is respectfully requested that this rejection be reconsidered and withdrawn.

Regarding the rejection of Claims 2 and 4 under 35 U.S.C. § 112, second paragraph, as allegedly being indefinite, this rejection is respectfully traversed in part, Claim 2 having been canceled and thus the rejection being rendered moot with respect thereto. Regarding Claim 4, it is alleged that it appears that there is no "tristate circuit" as set forth in this claim. It is respectfully pointed out that in Figure 1 the circuit elements XTRI, MP1, MN2, MN3 and MP3 serve in the tristate function, and are part of the tristate circuit of the embodiment shown in that figure. Their operation is described in the Specification at page 8, lines 3-9. Thus, a tristate circuit is disclosed and described in the Specification. While circuit elements MP1, MN2, MN3 and MP3 are depicted in the figure as merged with the respective upper or lower predriver circuit in the output circuit with respect to which they operate, their function in providing the tristate function is clearly disclosed and described. (It is noted that they could be shown in separate blocks, although it is believed that such an attempt could reduce the clarity of the description.) Thus, it is respectfully submitted that a tristate circuit is disclosed and shown in the Specification. Accordingly, it is respectfully requested that this rejection be reconsidered and withdrawn.

Regarding the rejection of Claim 1 under 35 U.S.C. § 102(b) as allegedly being anticipated by the patent to Bancal, Claim 1 has been canceled, thereby

rendering this rejection moot. Accordingly, it is respectfully requested that this rejection be reconsidered and withdrawn.

Regarding the rejection of Claims 1-4 under 35 U.S.C. § 103(a) as allegedly being unpatentable over the patent to Ten Eyck in view of the patent to Lin, this rejection is respectfully traversed in part, Claims 1 and 2 having been canceled and thus the rejection being rendered moot with respect thereto. Regarding Claims 3 and 4, independent Claim 3 sets forth an output circuit, and recites an upper damping control circuit branch, comprising a first resistor and a first diode connected in parallel between a first node and a second node, the second node being coupled to an output node, a lower damping control circuit branch, comprising a second resistor and a second diode connected in parallel between a third node and the second node, an upper output transistor coupled by its source and drain between a power supply and the first node, and having a gate and a lower output transistor coupled by its source and drain between ground and the third node, and having a gate. It has been admitted that the patent to Ten Eyck does not disclose that the claimed damping control circuits. Nor does it suggest such circuits. Thus, the patent to Ten Eyck does not anticipate or render obvious the invention as set forth in Claim 3.

The patent to Lin fails to cure the deficiencies of the patent to Ten Eyck. This patent apparently relates to a buffer for reducing voltage ringing and overshooting that is modified to improve electrostatic discharge (ESD) protection. Prior art to their arrangement was, for example, output buffer 18 in their Figure 1B, including resistor R_n in series with NMOS device N1 between an I/O pin pad and a "low power node" (ground? substrate?). The problem they seek to solve is that the presence of resistor R_n at the pad node degrades the performance of ESD protection. In their arrangement, one or more diodes are placed in parallel with resistor R_n, for example diode D1 as shown in their Figure 2. The function of diode D1 is to act as an open circuit during normal circuit operation, while allowing resistor R_n to suppress voltage ringing and overshoot as in the prior art. See Lin, column 4, lines 22-47, esp. lines 34-36. Thus, the patent to Lin fails to

show or describe a lower damping control circuit branch, comprising a second resistor and a second diode connected in parallel between a third node and the second node, and a lower output transistor coupled by its source and drain between ground and the third node, and having a gate. Lin's diode D1 and resistor R_n are not connected in parallel between a third node and an output node, wherein a lower output transistor is connected between the third node and ground, as recited in Claim 3, because their NMOS device N1 is not an output transistor as recited in Claim 3. Thus, the patent to Lin fails to cure the deficiencies of the patent to Ten Eyck.

The other art of record is even less relevant.

It is therefore respectfully submitted that neither the patent to Ten Eyck nor the patent to Lin, nor, indeed, any of the art of record, whether considered alone or in any combination, anticipate or render obvious the invention as set forth in Claim 3, and that therefore Claim 3 is allowable over the patent to Ten Eyck and the patent to Lin. Claim 4 depends from Claim 3 and so is allowable as well for the same reasons, as well as for the additional limitations found therein. Wherefore, reconsideration and withdrawal of this rejection are respectfully requested.

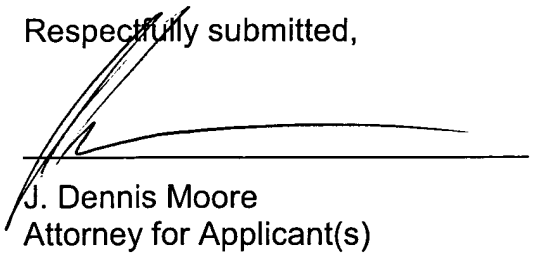
It is respectfully submitted that the claims recite the patentably distinguishing features of the invention and that, taken together with the above remarks, the present application is now in proper form for allowance. Reconsideration of the application, as amended, and allowance of the claims are requested at an early date.

While it is believed that the instant amendment places the application in condition for allowance, should the Examiner have any further comments or suggestions, it is respectfully requested that the Examiner contact the undersigned in order to expeditiously resolve any outstanding issues.

To the extent necessary, the Applicants petition for an Extension of Time under 37 C.F.R. §1.136. Please charge any fees in connection with the filing of

this paper, including extension of time fees to the Deposit Account No. 20-0668 of Texas Instruments Incorporated.

Respectfully submitted,



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